Abstract

Nowadays the use of commercial off-the-shelf (COTS) processors has become a common trend in safety-critical applications. Since the occurrence of the failure in these applications may result in catastrophic consequences such as loss or serious hurt to people, extreme harm to property and environmental scathe, the faults must be detected as soon as possible. The occurrence of transient and intermittent faults is 10 to 30 times more frequent than permanent faults, also up to 77% of the transient faults lead to the control flow errors. Therefore, it seems that control flow checking techniques are a viable solution to the processors reliability requirements. In this thesis two techniques are presented to detect and mask control flow errors. In the first technique, a hybrid method is proposed to detect control flow errors using performance counters. This method counts the number of instructions committed in a basic block and detects control flow errors. This method is able to detect 97.9% of injected faults while it had 115.6% performance overhead with 25.97% memory overhead. The main idea behind of the second technique in order to mask wrong-successor control flow errors, is to differentiate the control variables and applying a proper fault masking technique on them. The experimental results demonstrate that the proposed technique is able to mask all injected faults in control variables; while it had negligible performance and memory overheads.

Keywords: Fault Tolerance, Control Flow Error, Control Flow Checking, Performance Counters, Error Detection

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